CLAIMS

What is claimed is:

1. A semiconductor structure, comprising:

a substrate;

a patterned oxide layer disposed over the substrate;

a layer of undoped silicate glass disposed over the patterned oxide layer;

a layer of borophosphorous silicate glass over the layer of undoped silicate glass; and

a layer of plasma-enhanced tetraethyl orthosilicate over the layer of borophosphorous silicate glass, the layers of undoped silicate glass, borophosphorous silicate glass, and plasma-enhanced tetraethyl orthosilicate together forming a pre-metal dielectric stack.

2. The structure of claim 1 wherein the layer of borophosphorous silicate glass has a thickness between approximately 2k and 8k angstroms.

3. The structure of claim 1 wherein the layer of plasma-enhanced tetraethyl orthosilicate is planar.

4. The structure of claim 3 wherein a combined thickness of the oxide layer, the layer of undoped silicate glass, the layer of borophosphorous silicate glass, and the layer of plasma-enhanced tetraethyl orthosilicate is less than approximately 15k angstroms.

5. The structure of claim 3, further comprising a layer of tetraethyl orthosilicate disposed over the layer of plasma-enhanced tetraethyl orthosilicate.

6. An integrated circuit, comprising:

a substrate;

a dielectric layer disposed on the substrate;

a layer of undoped silicate glass disposed on the dielectric layer;

an unplanar layer of borophosphorous silicate glass disposed on the layer of undoped silicate glass; and

a planar dielectric layer disposed on the unplanar layer of borophosphorous silicate glass, the layers of undoped silicate glass, borophosphorous silicate glass, and planar dielectric together composing a pre-metal dielectric stack.

7. The integrated circuit of claim 6 wherein the planar dielectric layer comprises plasma-enhanced tetraethyl orthosilicate.

8. The integrated circuit of claim 6, further comprising a dielectric layer disposed on the planar dielectric layer.

9. The integrated circuit of claim 6, further comprising:

a layer of tetraethyl orthosilicate disposed on the planar dielectric layer; and

wherein the planar dielectric layer comprises plasma-enhanced tetraethyl orthosilicate.

10. The integrated circuit of claim 6, further comprising:

a layer of plasma-enhanced tetraethyl orthosilicate disposed on the planar dielectric layer; and

wherein the planar dielectric layer comprises plasma-enhanced tetraethyl orthosilicate.

11. A method for forming a semiconductor structure, the method comprising:

forming a patterned oxide layer over a substrate;

forming a USG layer on the patterned oxide layer and exposed portions of the substrate;

forming a BPSG layer on the USG layer;

forming a PE-TEOS layer over the BPSG layer; and

planarizing the PE-TEOS layer to form a pre-metal dielectric stack.

12. The method of claim 11 wherein the planarizing is accomplished by a chemical-mechanical polishing technique.

13. The method of claim 11, further comprising forming a TEOS layer on the planarized PE-TEOS layer.

14. The method of claim 11 wherein the BPSG layer is between approximately 2k to 8k angstroms thick.

15. The method of claim 11 wherein the USG layer is between approximately 1k to 4k angstroms thick.

16. The method of claim 11 wherein a total thickness of the oxide layer, the USG layer, the BPSG layer, and the planarized PE-TEOS layer is less than approximately 15k angstroms.

17. The method of claim 13 wherein the TEOS layer is between approximately 1k to 5k angstroms thick.

18. The method of claim 11, further comprising forming a PE-TEOS layer on the planarized PE-TEOS layer.

19. The method of claim 18 wherein the PE-TEOS layer is between approximately 1k to 5k angstroms thick.